









INTERNSHIP

1 WEEK TRAINING PROGRAMME FOR B.TECH STUDENTS ON

FPGA-BASED DIGITAL SYSTEM DESIGN USING VERILOG

What You'll Learn:

- · FPGA Architecture & Workflow
- Verilog HDL Programming
- · Digital Design & Simulation
- · Hands-on Lab Sessions
- · FPGA Project Implementation

Organised by: College of Engineering Attingal in association with Model Engineering College, Thrikkakara
(Managed by IHRD, Govt. of Kerala)

Under Chips to startup (C2S) Programme, MeitY, Govt. of India

Starts on 24th June 2025

Duration: 5 days

Who Can Attend? 4th, 6th & 8th semester B Tech Students of: EC, EV, EE, EB, EI and

allied branches

Why Join?

- · Practical, hands-on training
- Industry-relevant skill development
- · Certificate of completion
- · Expert mentorship

Program Fee:

₹2000/-+18% GST

Register at: https://forms.gle/U2xMHyLCpfXG3v8o8 Limited seats available! Register early to confirm your spot.



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